REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1 and 6-16 remain in the application. Claim 1 has been amended. Claims 2-5 and 17 have been cancelled.

In item 4 on pages 2-6 of the above-mentioned Office action, claims 1-15 and 17 have been rejected as being unpatentable over Nunziata (US 5,619,471) in view of Kerstein et al. (US 6,021,478) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in Fig. 1 of the drawings, page 10, line 25, to page 12, line 24, of the specification as well as original claims 2-5.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> receiving a control signal from outside the integrated memory unit with the external terminal pins;
>
> before a memory access, partitioning the memory cell field into a plurality of memory areas, the uniform size

of the memory areas or the number of the memory areas being dependent on the control signal.

Nunziata describes a memory system with a memory controller for operating a DRAM in either an interleaved or non-interleaved manner. Memory controllers are provided for determining how DRAM banks have been populated (for example with no chips, eight 256Kx4-bit DRAM chips, eight 1Mx4-bit DRAM chips or eight 4Mx4-bit DRAM chips). At initialization of the system, the microprocessor 10 surveys the DRAM using conventional software to determine the size of the DRAM banks, which populate each of those banks or to determine empty banks. The size information is then stored in a size register (see column 10, lines 1 to 8). If paired DRAM banks have been populated with the same size DRAM chips, then the memory controller will access those DRAM banks as interleaved. If, on the other hand, paired DRAM banks are populated with different size DRAM chips or if only one bank of the pair is populated, then the memory controller operates on these banks in a non-interleaved fashion (see column 2, lines 43 to 56).

Kerstein et al. describe a method for operating a microprocessor and a burst memory using a chip enable and an output enable signal. In accordance with the method prior to Kerstein et al., the burst transfer begins when the memory receives a dedicated control signal (BURST) from the CPU

indicating that the next operation will be a burst transfer. The burst transfer terminates when the memory receives another dedicated control signal (BDIP) which indicates that the next subsequent data bit or word is the last data of the burst transfer (see column 1, lines 47 to 53). In accordance with the method of Kerstein et al., a memory device can be configured so that following the address phase, if the output enable pin has been activated for more than one consecutive clock cycle, the memory will initiate a burst transfer sequence. If the output enable pin is deactivated prior to the next address phase requested from the CPU, burst transfer will be suspended until the output enable pin is activated again. If the CPU requests a different address phase (chip enable activated) from the memory while the output enable is activated, a current burst transfer will be terminated and the next memory cycle will begin. Existing memory chip enable (CE) and output enable (OE) pins for controlling bursting of data are used instead of requiring the use of dedicated or special burst control pins, such as BURST or BDIP (see column 2, lines 13 to 41).

The invention of the instant application makes it possible to reduce a high number of required external terminal connections or pins in that a memory area address for a memory access and, subsequently one after the other, access data of the relevant

memory areas, are transmitted through at least one common external terminal connection of the memory unit. An initialization of the memory unit is carried out before a memory access. The memory cell field is partitioned into a number of memory areas, each of which has the same size, during the initialization step. For such a purpose, the number of memory areas is transmitted through terminal connections I/Os 1 to 4, from which results the size of each of the memory areas, which are all of equal size. Alternatively, the size of one memory area is transmitted through terminal connections, for which the number of memory areas to be defined would result.

For the memory access, a memory area address BADR is applied to I/Os 1 to 9 for selecting one of the memory areas for a read or write access. Subsequently, a start address SADR is transmitted through terminal connections I/Os 1 to 14 to select a memory cell inside the selected one of the memory areas for the read or write access. Starting from such a start address SADR, addresses ADR are generated by a counter Z for the access to memory cells of the selected one of the memory areas. A defined number of cycles later, the write data are provided at the I/Os and are taken over by the chip. Write data are thereby transmitted successively in a rapid sequence.

If the internal address counter has reached the end of the selected one of the memory areas, the write cycle will be terminated. If it is not desired to run through all addresses up to the end of the selected one of the memory areas, an interrupt command is transmitted for the interruption or termination of the memory access at a time defined by the interrupt command (see Fig. 1 and page 10, line 25 to page 12, line 24 of the specification).

In contrast to the invention of the instant application, neither Nunziata nor Kerstein et al. teach <u>distributing or partitioning</u> the memory cell field into a plurality of memory areas in dependence on a control signal which is applied to the external terminal pins. Nunziata teaches <u>surveying or determining</u> the size of the DRAM banks by the microprocessor (see column 10, lines 3 to 8). The size of each of the DRAM banks is dependent only on how the banks are populated by the manufacturer and not dependent on a partitioning action carried out by the microprocessor. Different bank configurations are presented in Nunziata (see column 4, lines 13 to 37). The microprocessor determines the capacity of the DRAM banks because it operates on paired banks in an interleaved or non-interleaved manner in dependence on the size of the DRAM chips (see column 4, lines 35 to 48). That means that the surveying step of the DRAM banks by the

microprocessor is only a kind of passive measuring or surveying step, which does not change the partitioning of the banks.

In the invention of the instant application, the size of the memory cell field is not surveyed by a microprocessor, but is distributed or partitioned in a number of memory areas in dependence on the control signal, which is transmitted through external terminal connections I/Os 1 to 4 (see page 11, line 25 to page 12, line 8 of the specification).

In conclusion, neither Nunziata nor Kerstein et al. teach partitioning a memory cell field into a number of memory areas in dependence on a control signal transmitted through external terminal pins.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well. Claims 2-5 and 17 have been cancelled.

In view of the foregoing, reconsideration and allowance of claims 1 and 6-16 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Yonghong Chen

Yonghong Chen
Reg. No. 56,150

For Applicant

YC

March 3, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101